Amendments to the claims:

1. (Currently Amended) A circuit for input side impedance matching of a power amplifier in an electronic device, comprising:

a source for providing a signal, wherein the signal has a predetermined impedance; and

an impedance transformer network ~~to synthesize the predetermined impedance at an input of the power amplifier~~;

wherein the predetermined impedance of the signal is synthesized at an input of the power amplifier solely by the impedance transformer network, and wherein the entire impedance transformer network is joined in parallel with the source, and comprises a negative resistor in series with an inductor.

2. (Original) The circuit of claim 1, wherein the inductor has a reactance equal to a capacitance of the device at a required frequency of operation.

3. (Original) The circuit of claim 1, wherein the inductor is a bondwire inductor.

4. (Original) The circuit of claim 1, wherein a value of the negative resistor is selected to synthesize the predetermined impedance at an input of the power amplifier.

5. (Original) The circuit of claim 4, wherein the value of the negative resistor is approximately –7.4 Ohms.

6. (Original) The circuit of claim 4, wherein the predetermined impedance is approximately 50 Ohms.

7. (Original) The circuit of claim 4, wherein a normalized phase of the synthesized impedance is between approximately –0.5 to 0.5 Radians.

8. (Original) The circuit of claim 7, wherein the normalized phase is approximately –0.4 Radians.

9. (Original) The circuit of claim 1, wherein a ratio of signal voltage at an input of the power amplifier to signal voltage at the source is approximately 0.62.

10. (Currently Amended) A circuit for input side impedance matching of a power amplifier in an electronic device, comprising:

a source for providing a signal, wherein the signal has a predetermined impedance;

an impedance transformer network ~~to synthesize~~ solely by which the predetermined impedance at an input of the power amplifier is synthesized, said entire impedance transformer network being joined in parallel with the source and comprising a negative resistor in series with an inductor;

wherein a value of the negative resistor is selected to synthesize the predetermined impedance at an input of the power amplifier, and wherein the inductor has a reactance equal to a capacitance of the device at a required frequency of operation.

11. (Original) The circuit of claim 10, wherein the predetermined impedance is

approximately 50 Ohms, and wherein the value of the negative resistor is approximately –7.4 Ohms.

12. (Original) The circuit of claim 11, wherein the synthesized impedance has a normalized phase between approximately –0.5 and 0.5 Radians.

13. (Original) The circuit of claim 12, wherein the normalized phase is approximately –0.41 Radians.

14. (Original) The circuit of claim 13, wherein a ratio of signal voltage at the input to signal voltage at the source is approximately 0.62.

15. (Currently Amended) A method for matching impedance at an input of a power amplifier in an electronic device, comprising the steps of:

providing a signal from a source, wherein the provided signal has a predetermined impedance;

joining an impedance transformer network, solely by which the predetermined impedance is synthesized at an input of the power amplifier, in parallel in its entirety with the source ~~to synthesize the predetermined impedance at an input of the power amplifier~~, wherein the network comprises a negative resistor in series with an inductor; and

selecting a value for the negative resistor so that the predetermined impedance is synthesized at the input of the power amplifier.

16. (Original) The method of claim 15, further comprising the step of setting a

reactance of the inductor equal to a capacitance of the device at a required frequency of operation.

17. (Original) The method of claim 15, wherein the selecting step comprises selecting a value of –7.4 Ohms for the negative resistor.

18. (Original) The method of claim 15, wherein the predetermined impedance is approximately 50 Ohms.

19. (Original) The method of claim 15, wherein a normalized phase of the synthesized impedance is approximately –0.41 Radians.

20. (Original) The method of claim 15, wherein a ratio of signal voltage at the input to signal voltage at the source is approximately 0.62.